Electronic Version
Stylesheet Version v1.1.1

CHIP-PACKAGING WITH BONDING OPTIONS CONNECTED TO A PACKAGE SUBSTRATE

Abstract

A chip-packaging includes a package substrate, a chip, and a lead frame. The chip having a plurality of bonding pads is mounted on the package substrate. One of these bonding pads is connected to the package substrate. The package substrate has a GND voltage or a POWER voltage. The lead frame is connected to one bonding pad. With connection of these bonding pads with the lead frame and connection of these bonding pads with the package substrate, input ends or output ends in the chip could be connected to a GND voltage, a POWER voltage, and signal pins of the chip-packaging.